【ABSTRACT OF THE DISCLOSURE】

【Abstract】

To prevented boron ions from infiltrating a silicon wafer when a BPSG layer as a pre-metal dielectric layer is deposited, the BPGS layer is deposited after hydrogen of a surface of a liner nitride layer is removed by a ultraviolet ozone treatment of the surface of the liner nitride layer. The liner nitride layer is deposited as a lower layer before depositing the BPGS layer. The liner nitride layer prevents impurities such as boron, phosphorous, and others which are contained in a BPSG layer from infiltrating the silicon wafer including the MOS transistor when the BPSG layer as a pre-metal layer to be deposited at a subsequent process directly contacts the silicon wafer. The liner nitride layer also acts as an etch stop layer during later etching of BPSG layer to form contact holes.

Boron ions are previously prevented from infiltrating a silicon wafer by preventing generation of boron ions by reaction between hydrogen on the surface of the liner nitride layer and B-O of the BPGS layer. Accordingly, degradation of a semiconductor device is prevented by preventing a reduction of a threshold voltage of a PMOS and current leakage.

【Representative Drawing】

FIG. 2c

【Key Word】

pre-metal dielectric layer, liner nitride layer, BPSG, ultraviolet ozone treatment

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【SPECIFICATION】

【TITLE OF THE INVENTION】

METHOD FOR MANUFACTURING PRE-METAL DIELECTRIC LAYER OF SEMICONDUCTOR DEVICE

【BRIEF DESCRIPTION OF THE DRAWINGS】

FIGS. 1a and 1b are schematic process drawings of a conventional method for manufacturing a pre-metal dielectric layer of a semiconductor device.

FIGS. 2a to 2c are schematic process drawings of a method for manufacturing a pre-metal dielectric layer of a semiconductor device according to an exemplary embodiment of the present invention.

【DETAILED DESCRIPTION OF THE INVENTION】

【Object of the Invention】

【Field of the invention and description of the related art】

The present invention relates to a process for manufacturing a semiconductor device. More particularly, the present invention relates to a method for manufacturing a pre-metal dielectric layer of a semiconductor device in a process for manufacturing a semiconductor device. The pre-metal dielectric layer is formed to electrically insulate between a silicon wafer that the semiconductor device is formed on, and a metal interconnect line layer.

Generally, a pre-metal dielectric layer is formed of an oxide layer to electrically insulate between a silicon wafer that the semiconductor device is formed on, and a metal interconnect line layer. A BPSG (borophosphosilicate glass) layer of SiO_2-B_2O_3-P_2O_5 is formed by adding a reactant having boron or phosphorous to planarize the metal interconnect line layer when the oxide layer is formed and for gettering of sodium ion (Na+) and others.

A conventional method for manufacturing a pre-metal dielectric layer of a semiconductor device will be described with reference to FIGS. 1a and 1b.

Referring first to FIG. 1a, a MOS transistor 3 including a gate oxide layer and a gate G, a source S, and a drain D that are formed of poly silicon is formed at a device region of a silicon wafer 1. A device isolation region is defined on the silicon wafer 1 by a field oxide layer 2 formed by a LOCOS (local oxidation of silicon) process, an STI (shallow trench isolation) process, or others. In addition, silicide 4 is formed over a surface of the gate G, the source S, and the drain D to reduce contact resistance between the gate G, the drain D, and the source, and a metal interconnect line layer to be formed in a subsequent process. Subsequently, a liner nitride layer 5 is deposited over the entire surface of the silicon wafer 1 including the MOS transistor 3. The nitride layer 5 prevents impurities such as boron, phosphorous, and others which are contained in a BPSG layer from infiltrating the silicon wafer 1 including the MOS transistor 3 when the BPSG layer as a pre-metal layer to be deposited in a subsequent process directly contacts the silicon wafer 1. The liner nitride layer 5 also acts as an etch stop layer during later etching of the BPSG layer to form contact holes.

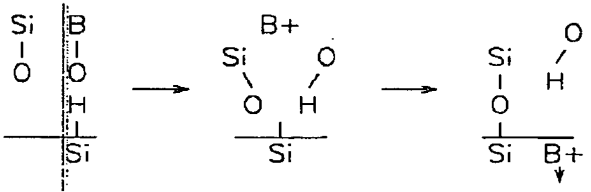
Subsequently, as shown in FIG. 1b, a TEOS (tetraethylorthosilicate) type of BPSG layer 6 as a pre-metal layer is deposited over the entire surface of the liner nitride layer 5 to a thickness of about 14,000Å by an APCVD (atmospheric pressure chemical vapor deposition) method or an SACVD (sub-atmospheric chemical vapor deposition) method. Here, with respect to the deposited BPSG layer 6, the bonds between B-O, P-O, and Si-O are weak such that they are easily broken by external chemical and mechanical contact. Therefore, a densification process is performed at a temperature of about 700°C to obtain a stable BPSG layer 6. The chemical and mechanical strength of the BPSG layer 6 is increased by approximately three times by the densification process as compared with before the densification process. After this, a pre-metal layer of the semiconductor is completed by planarization of the BPSG layer 6.

In the conventional method, a PECVD (plasma enhanced chemical vapor deposition) method using plasma and low temperature, an LPCVD (low pressure chemical vapor deposition) method using low pressure and high temperature, or other methods may be used to form the liner nitride layer 5. In particular, the PECVD method has been generally used in recent years because a low temperature process is possible. The liner nitride layer 5 that is deposited by a reaction of silane (SiH4) and ammonia (NH3) according to the PECVD method is less stoichiometric than the liner nitride layer that is deposited by the LPCVD method. Because of this, as shown in A1 of FIG. 1b, PECVD of the liner nitride layer 5 has plentiful hydrogen (H) (about 20 to 30 mole%; the hydrogen content by LPCVD method is 4 to 6 mole%.) that is generated in the decomposition process of silane and ammonia. Existence shapes are various as follows: $Si-H$, $Si-H_2$, $Si-H_3$, $N-H$, $N-H_2$, and others. These exist not only inside of the layer but also at the surface of the liner nitride layer 5, and a bonding force of Si-H among these bonds is very weak such that it is easily broken by external chemical contact. Here, a chemical structure at an interface of the liner nitride layer 5 and the BPSG layer 6 in the case that the BPSG layer

6 is formed over the liner nitride layer is shown in A1 of FIG. 1b.

Additionally, in the case that the BPSG layer 6 is deposited over the liner nitride layer 5, as shown in Reaction Formula 1, Si-H of the surface of the liner nitride layer 5 and in the vicinity thereof contacts unstable B-O, P-O, and Si-O of the deposited BPSG layer 6. At this time, thermal energy from a deposition temperature of about 400°C to 500°C of the BPSG layer 6 is received. The bonding force of Si-H is further weakened by the thermal energy, and Si-H contacts and easily reacts to B-O, P-O, and Si-O in this state. The reaction is achieved to stabilize them, and hydrogen on the surface of the liner nitride layer 5 and oxygen of B-O are combined and stabilized and B-O, P-O, or Si-O is positioned at the location where hydrogen is removed. Finally, only boron ions (B+) are left over when oxygen is removed, and the boron ions infiltrate the liner nitride layer 5 because of its small atomic radius and excellent mobility, or remains inside the liner nitride layer 5. The above case may be generated at B, P, or Si, but P and Si cannot infiltrate the liner nitride layer 5 because P and S have large atomic radii and mobility of P and Si is substantially lower than that of B.

【Reaction Formula 1】



Further, the BPSG layer 6 is densified by a heat treating process when the BPSG layer 6 is deposited. At this time, boron ions that remain inside the liner nitride layer 5 or that have infiltrated the liner nitride layer 5 infiltrate the silicon wafer 1.

The boron ions infiltrated in this manner particularly generate problems in the PMOS using boron as impurities of the source S and the drain D. The infiltrated boron ions reduce the threshold voltage of the PMOS by moving in the silicon and cause current leakage. A channel may be poorly formed by the current leakage even when an applied voltage is removed to remove the gate channel.

【Object to be achieved by the present invention】

The present invention has been made to solve the above-noted problem, and an objective of the present invention it to prevent boron ions from infiltrating the silicon wafer when a BPSG layer as a pre-metal dielectric layer of a semiconductor device is deposited.

【Constitution and Operation of the Invention】

In order to achieve the objective, after hydrogen of a surface of a liner nitride layer is removed by ultraviolet ozone treatment of the surface of the liner nitride layer that is deposited by PECVD, a BPGS layer is deposited so boron ions are not formed in the present invention.

That is, the present invention comprises a step of forming a semiconductor device having a gate, a source, and a drain at a device region of a silicon wafer, a device isolation region is defined on the silicon wafer, a step of depositing a liner nitride layer over the entire surface of the silicon wafer including the semiconductor device by a PECVD method, a step of performing ultraviolet ozone treatment to a surface of the liner nitride layer to remove hydrogen from the surface of the liner nitride layer and the vicinity thereof, and a step of forming a BPSG layer as a pre-metal layer over the entire surface of the liner nitride layer and densifying the BPSG layer.

The silicon wafer in which the liner nitride layer is deposited is put in a chamber with an ozone atmosphere and ultraviolet rays are irradiated thereto for 40 seconds to 80 seconds in the step of performing ultraviolet ozone treatment to the surface of the liner nitride layer.

It is preferable that ozone gas flows into the chamber at a flow rate of 5000cc/min to 7000cc/min to form the ozone atmosphere.

it is preferable that the ultraviolet rays are irradiated using an ultraviolet lamp and that a temperature of the silicon wafer is 300°C to 400°C during the step of performing ultraviolet ozone treatment to a surface of the liner nitride layer.

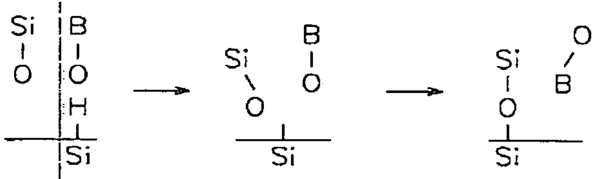
A preferable embodiment of the present invention will now be described in detail with reference to the accompanying drawings.

FIGS. 2a to 2c are schematic process drawings of a method for manufacturing a pre-metal dielectric layer of a semiconductor device according to an exemplary embodiment of the present invention.

Firstly, as shown in FIG. 2a, a transistor device, for example a MOS transistor 13, including a gate oxide layer and a gate G, a source S, and a drain D that are formed of poly silicon is formed at a device region of a silicon wafer 11. A device isolation region is defined on the silicon wafer 11 by a field oxide layer 12 formed by a LOCOS (local oxidation of silicon) process, an STI (shallow trench isolation) process, or other processes. At this time, sidewalls are formed to both sides of the gate G, and the source S and the drain D may be formed of an LDD structure. Also, silicide 14 is formed on an upper surface of the gate G, the source S, and the drain D to reduce contact resistance between the gate G, the drain D, and the source S and a metal interconnect line layer to be formed in a subsequent process. Subsequently, a liner nitride layer 15 as a lower layer is deposited over the entire surface of the silicon wafer 11 including the MOS transistor 13. The liner nitride layer 15 prevents impurities such as boron, phosphorous, and others which are contained in a BPSG layer from infiltrating the silicon wafer 11 including the MOS transistor 13 when the BPSG layer as a pre-metal layer to be deposited in a subsequent process directly contacts the silicon wafer 11. The liner nitride layer 15 also acts as an etch stop layer during later etching of the BPSG layer to form contact holes. At this time, the liner nitride layer 15 is deposited to a thickness of about 250Å to 350Å by a PECVD method at a certain temperature, for example, about 350°C to 450°C, using silane and ammonia. The deposited liner nitride layer 15 has plentiful hydrogen of about 20 to 30 mole% that is generated during a decomposition process of silane and ammonia. Existence shapes are various as follows: Si-H, $Si\text{-}H_2$, $Si\text{-}H_3$, N-H, $N\text{-}H_2$, and others. These maintain their bonds not only inside the nitride layer 15 but also at a surface of the liner nitride layer 15, and a bonding force of Si-H among these bonds is very weak such that it is easily broken by external chemical contact.

Subsequently, as shown in FIG. 2b, an ultraviolet ozone (O_3) treatment T is performed on the surface of the liner nitride layer 15 having hydrogen in great quantities. That is, the silicon wafer in which the liner nitride layer 15 is formed is put in a chamber for the ultraviolet ozone treatment T, and ozone gas is flowed over the silicon wafer 11 (preferably, over the liner nitride layer 15) at a flow rate of 5000cc/min to 7000cc/min, as an example, to form the ozone atmosphere. Ultraviolet rays are irradiated thereto for 40 seconds to 80 seconds, as an example. In this case, the ultraviolet rays may be irradiated using an ultraviolet irradiation apparatus including an ultraviolet lamp. Also, it is preferable that the temperature of the silicon wafer is 300°C to 400°C. Then, ozone is decomposed into O_2 and O by irradiation of the ultraviolet rays and the heat. O between these chemically reacts at the surface of the liner nitride layer 15 such that hydrogen having a weak bond on the surface of the liner nitride layer 15 and in the vicinity therefore is removed according to Reaction Formula 2. The hydrogen is replaced with oxygen, and the place where the hydrogen is removed at the surface of the liner nitride layer 15 and in the vicinity thereof is ionized and thus reactivity is increased.

【Reaction Formula 2】



Subsequently, as shown in FIG. 2c, a TEOS type of BPSG layer 16 as a pre-metal dielectric layer is deposited to a thickness of about 12,000Å to 16,000Å by an APCVD method or an SACVD method over the entire surface of the liner nitride layer 15 and the vicinity thereof having high reactivity, by ultraviolet ozone treatment T. Then, as shown in A11 of FIG. 2c, the surface of the liner nitride layer 15 is easily filled with B-O, P-O, and Si-O, and a relatively strong covalent bond is formed according to Reaction Formula 2. At this time, with respect to the BPSG layer 16, the bonds between B-O, P-O, and Si-O are weak such that they are easily broken by external chemical and mechanical contact. Therefore, a densification process is performed at a temperature of about 600°C to 800°C to obtain a stable BPSG layer 16. Therefore, the chemical and mechanical strength increases by approximately three times by the densification process as compared with before the densification process. Also, B-O is further stabilized similar to B_2O_3 by receiving the heat. After this, a pre-metal layer is completed by planarization of the BPSG layer 6 of the semiconductor device.

【Effect of the Invention】

As can be seen from the above description, according to the present invention boron ions are prevented from infiltrating a silicon wafer by preventing generation of boron ions by reaction between hydrogen on the surface of a liner nitride layer and B-O of a BPGS layer. Accordingly, degradation of a semiconductor device is prevented by preventing a reduction of a threshold voltage of a PMOS and current leakage. This is because a BPGS layer is deposed after hydrogen of a surface of a liner nitride layer is removed by ultraviolet ozone treatment of the surface of the liner nitride layer. The liner nitride layer is deposited as a lower layer before depositing the BPGS layer. The liner nitride layer prevents impurities such as boron, phosphorous, and others which are contained in a BPSG layer from infiltrating the silicon wafer including the MOS transistor when the BPSG layer as a pre-metal layer to be deposited at a subsequent process directly contacts on the silicon wafer. The liner nitride layer also acts as an etch stop layer during later etching of the BPSG layer to form contact holes.

【CLAIMS】

【Claim 1】

A method for manufacturing a pre-metal dielectric layer of a semiconductor device, comprising:

a step of forming a semiconductor device having a gate, a source, and a drain at a device region of a silicon wafer, a device isolation region being defined on the silicon wafer;

a step of depositing a liner nitride layer over an entire surface of the silicon wafer including the semiconductor device by a PECVD method;

a step of performing ultraviolet ozone treatment to a surface of the liner nitride layer to remove hydrogen from the surface of the liner nitride layer and the vicinity thereof; and

a step of forming a BPSG layer as a pre-metal layer over the entire surface of the liner oxide layer and densifying the BPSG layer.

【Claim 2】

The method of claim 1, wherein the silicon wafer on which the liner nitride layer is deposited is put in a chamber with an ozone atmosphere and ultraviolet rays are irradiated thereto for 40 seconds to 80 seconds in the step of performing ultraviolet ozone treatment to the surface of the liner nitride layer.

【Claim 3】

The method of claim 2, wherein ozone gas flows into the chamber at a flow rate of 5000cc/min to 7000cc/min to form the ozone atmosphere.

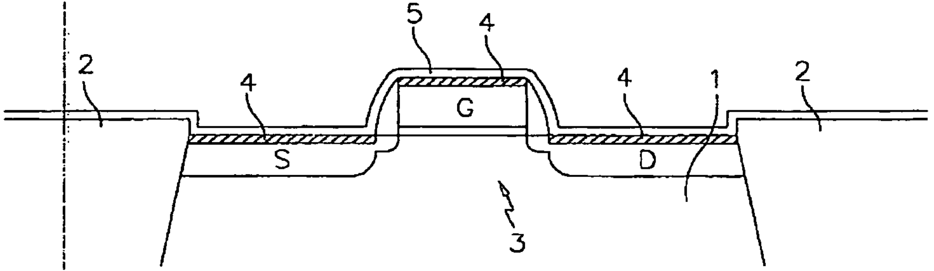
【Claim 4】

The method of claim 2 or claim 3, wherein the ultraviolet rays are irradiated using an ultraviolet lamp.

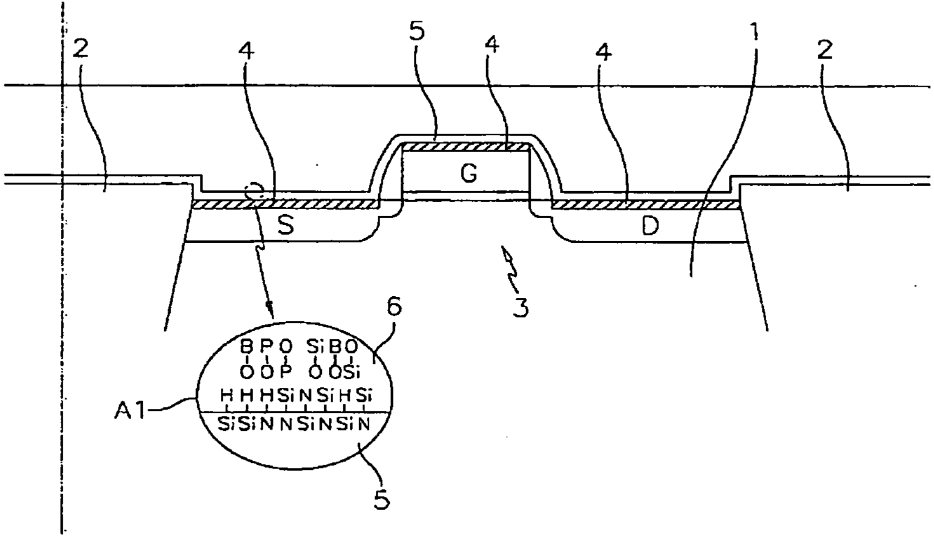
【Claim 5】

The method of claim 4, wherein the temperature of the silicon wafer is 300°C to 400°C during the step of performing ultraviolet ozone treatment to the surface of the liner nitride layer.

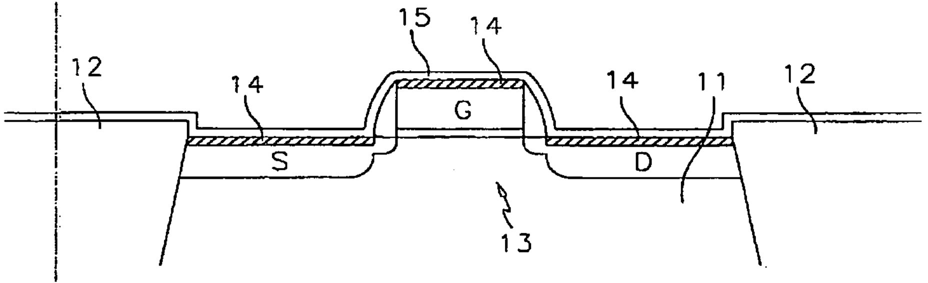
【FIG. 1a】



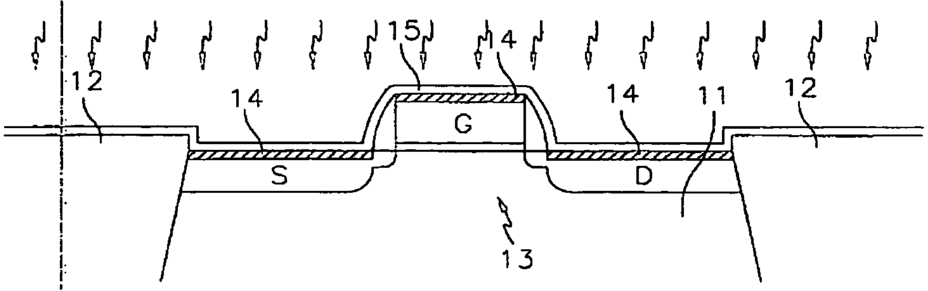
【FIG. 1b】



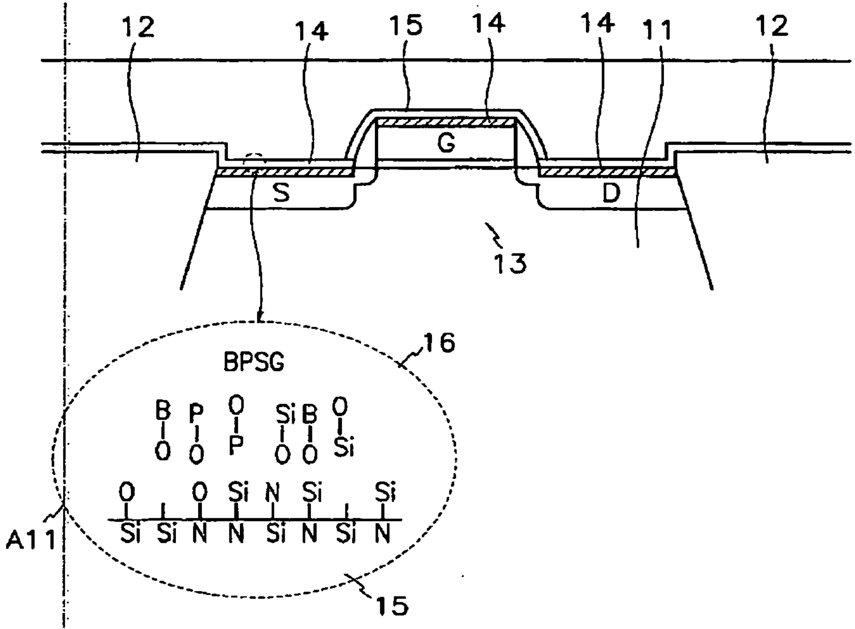
【FIG. 2a】



【FIG. 2b】


G
S
D

【FIG. 2c】


12
14
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BPSG
B P O Si B O
O O P O O Si
O O Si N Si Si
Si Si N N Si N Si N
A11
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